Future Technology
Devices International Ltd.

VINCULUM

BINDING USB TECHNOLOGIES

VDrive2

Vinculum VNC1L Module

http://www.vinculum.com

1. Introduction and Features

1.1 Introduction

The VDrive2 module provides an easy solution for adding a USB Flash disk interface to an existing product. Only four signal lines plus 5V supply and ground are required to be connected. Using the Vinculum VDAP firmware the VNC1L's I/O interface can be selected between the serial UART or SPI using the on-board jumper pins. Not only is the VDrive2 ideal for evaluation and development of VNC1L designs, but also its neat enclosure and attractive quantity discount structure makes this module suitable for incorporation into finished product designs. The VDrive2 is ideal for commercial products such as domestic goods, set top box, etc., as well as industrial products such as data loggers, software upgradable products, etc.

The Vinculum VNC1L is the first of F.T.D.I.'s Vinculum family of Embedded SoC USB host controller integrated circuit devices. Not only is it able to handle the USB Host Interface, and data transfer functions but owing to the inbuilt MCU and embedded Flash memory, Vinculum can encapsulate the USB device classes as well. When interfacing to mass storage devices such as USB Flash drives, Vinculum also transparently handles the FAT file structure communicating via UART, SPI or parallel FIFO interfaces via a simple to implement command set. Vinculum provides a new cost effective solution for providing USB Host capability into products that previously did not have the hardware resources available.

1.2 Features

- Uses F.T.D.I.'s VNC1L embedded USB host controller I.C. device.
- USB 'A' type socket to connect USB Flash disk.
- Traffic indicator LED.
- 2 mm (0.08") pitch 8 pin connector.
- 8-way header interconnect cable provided.
- Only four signals to connect, excluding power and ground.
- Jumper selectable UART or SPI interfaces.
- Single 5V supply input.
- Uses Vinculum VDAP firmware and command set.
- Enclosure with snap in place clips allows for easy front panel mounting.
- Program or update firmware via USB Flash disk or via UART interface.
- VNC1L firmware programming control pins PROG# and RESET# brought out onto internal jumper interface (only accessible on internal module PCB)
- VDrive2 is a Pb-free, RoHS complaint development module.
- Schematics, and firmware files available for download from the Vinculum website.

2. Pin Out

2.1 VDrive2 Pin Out

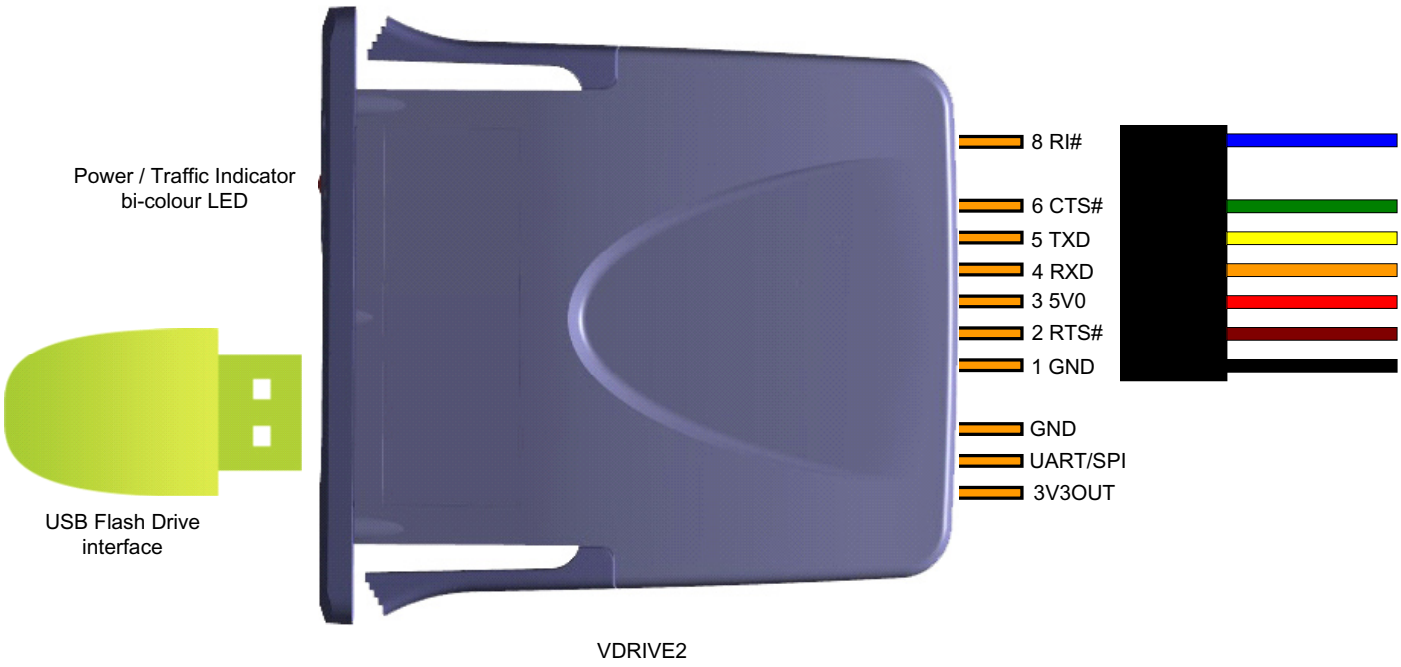


Figure 1 - VDrive2 Pin Out - UART interface.

Table 1 - Port Selection Jumper Pins

UART/SPI	I/O Mode
Pull-Up	Serial UART
Pull-Down	SPI

2.2 UART Interface Signal Descriptions

Table 2 - Data and Control Bus Signal Mode Options - UART Interface

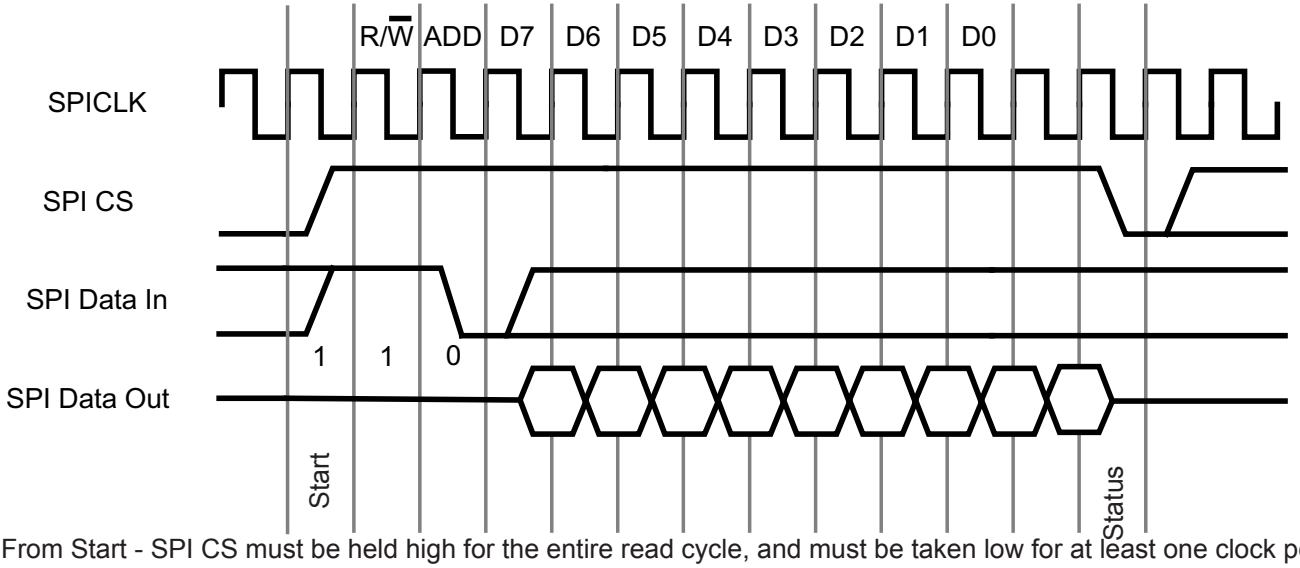
Pin No.	Name	Type	Description
1	GND	PWR	Signal ground
2	RTS#	Output	Request To Send Control Output / Handshake signal
3	5V0	PWR	5V supply input
4	RXD	Input	Receive asynchronous data input
5	TXD	Output	Transmit asynchronous data output
6	CTS#	Input	Clear To Send Control Input / Handshake signal
7	NC	-	No Connect
8	RI#	Input	Ring Indicator Control Input. Used to resume the Vinculum from suspend.

2.3 SPI Interface Signal Descriptions and Timing Diagrams

Table 3 - Data and Control Bus Signal Mode Options - SPI Interface

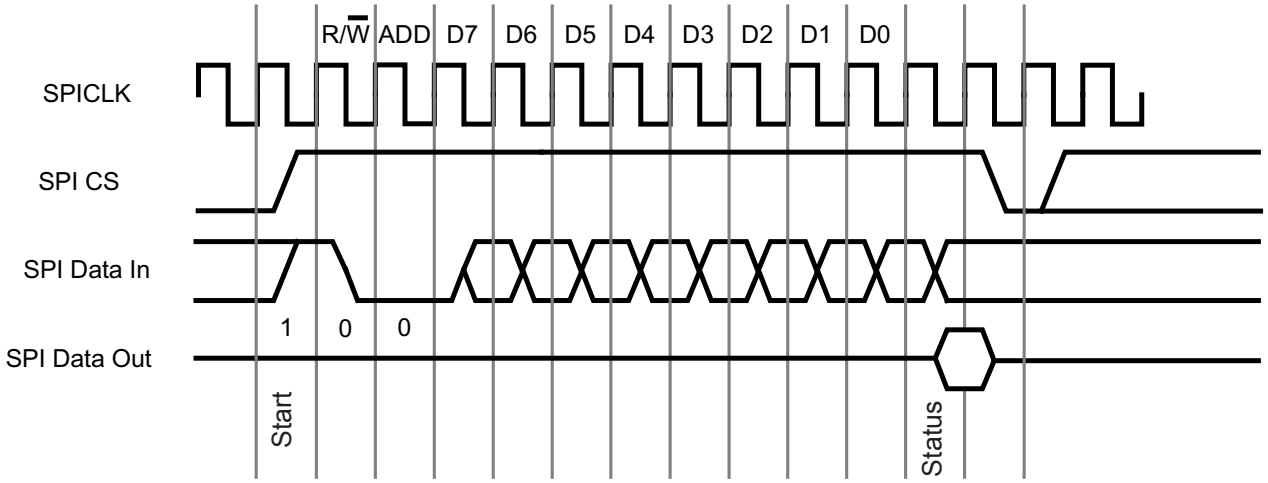
Pin No.	Name	Type	Description
5	SCLK	Input	SPI Clock input, 12MHz maximum.
4	SDI	Input	SPI Serial Data Input
2	SDO	Output	SPI Serial Data Output
6	CS	Input	SPI Chip Select Input

Figure 2 - SPI Slave Data Read Cycle



From Start - SPI CS must be held high for the entire read cycle, and must be taken low for at least one clock period after the read is completed. The first bit on SPI Data In is the R/W bit - inputting a '1' here allows data to be read from the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status register ('1') is read from. During the SPI read cycle a byte of data will start being output on SPI Data Out on the next clock cycle after the address bit, MSB first. After the data has been clocked out of the chip, the status of SPI Data Out should be checked to see if the data read is new data. A '0' level here on SPI Data Out means that the data read is new data. A '1' indicates that the data read is old data, and the read cycle should be repeated to get new data. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

Figure 3 - SPI Slave Data Write Cycle



From Start - SPI CS must be held high for the entire write cycle, and must be taken low for at least one clock period after the write is completed. The first bit on SPI Data In is the R/W bit - inputting a '0' here allows data to be written to the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status register ('1') is written to. During the SPI write cycle a byte of data can be input to SPI Data In on the next clock cycle after the address bit, MSB first. After the data has been clocked in to the chip, the status of SPI Data Out should be

checked to see if the data read was accepted. A ‘0’ level on SPI Data Out means that the data write was accepted. A ‘1’ indicates that the internal buffer is full, and the write should be repeated. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

Figure 4 - SPI Slave Data Timing Diagrams

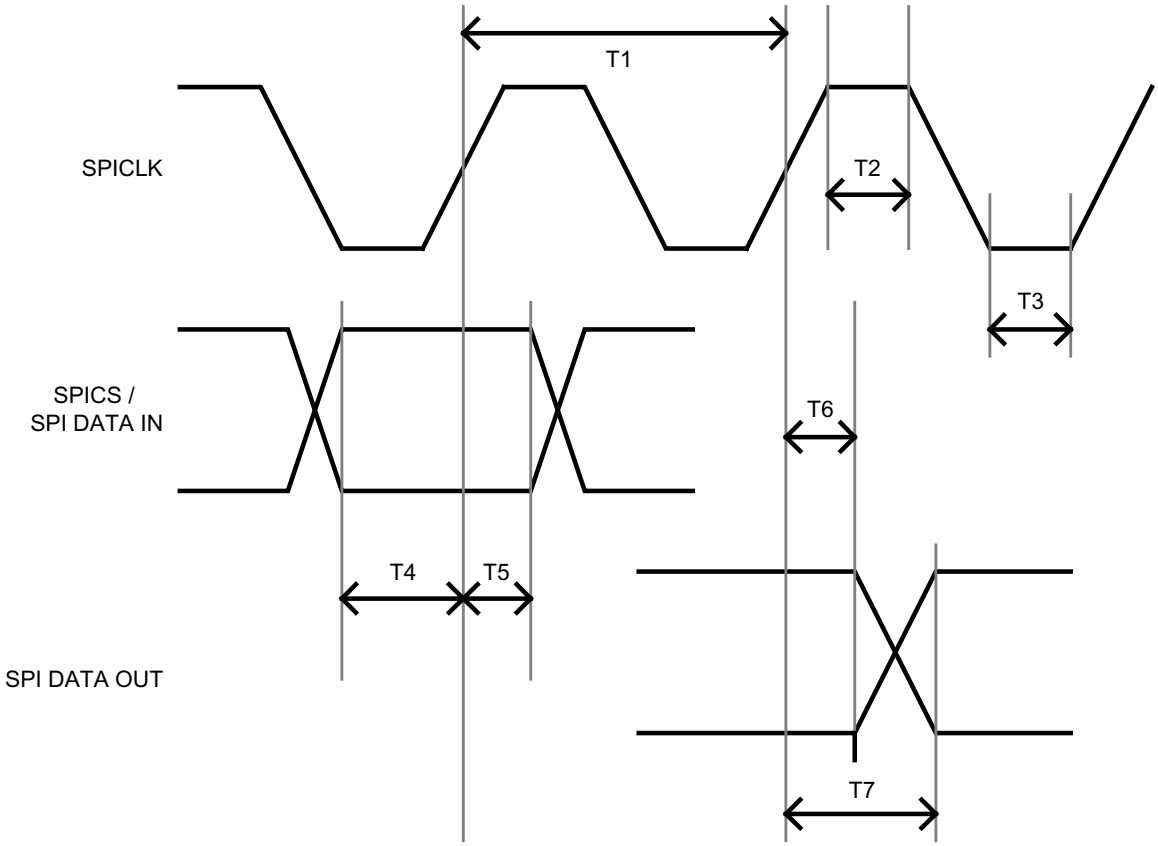


Table 4 - SPI Slave Data Timing

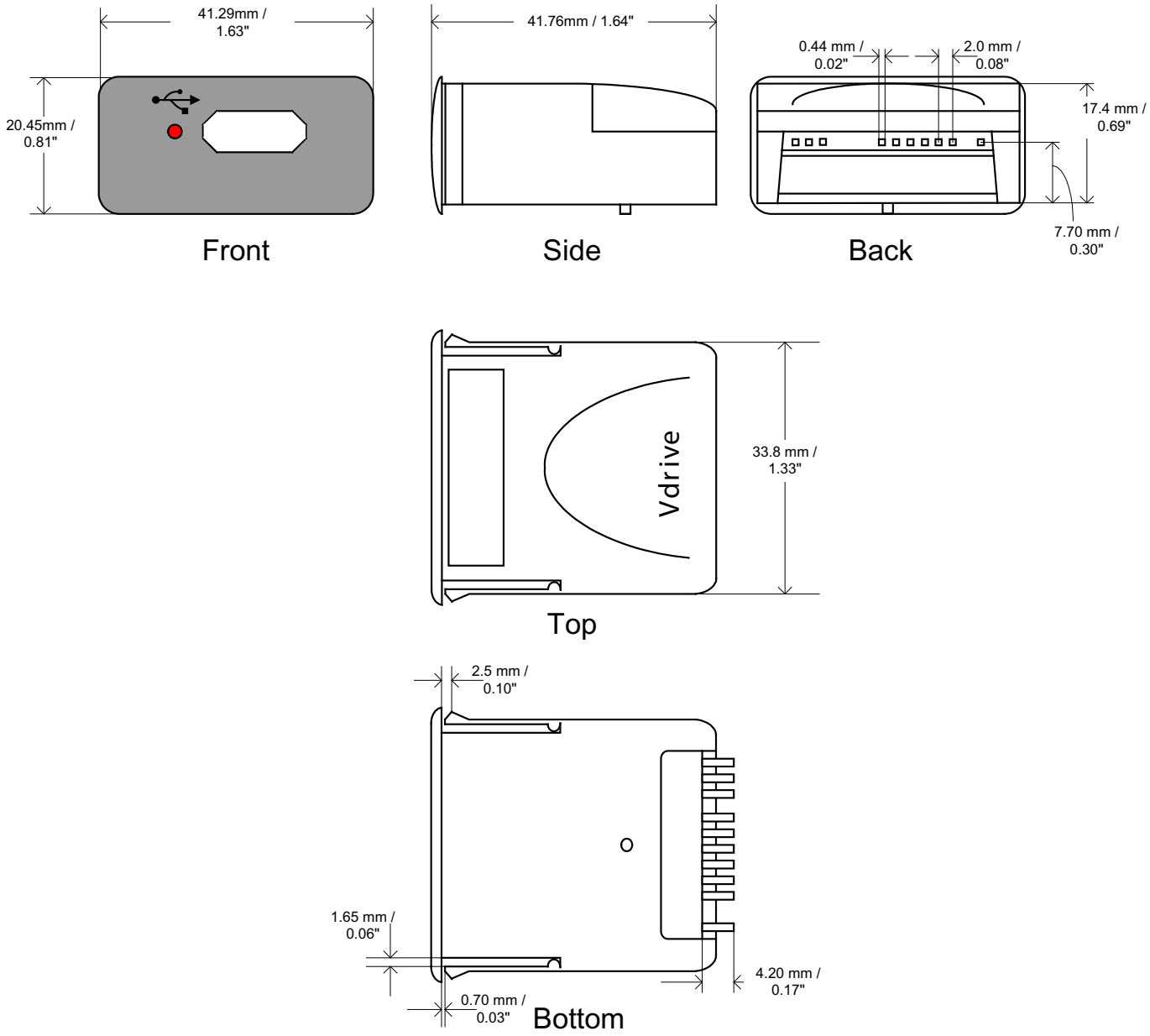
Time	Description	Min	Typical	Max	Unit
T1	SPICLK Period	83	-	-	ns
T2	SPICLK High	20	-	-	ns
T3	SPICLK Low	20	-	-	ns
T4	Input Setup Time	10	-	-	ns
T5	Input Hold Time	10	-	-	ns
T6	Output Hold Time	2	-	-	ns
T7	Output Valid Time	-	-	20	ns

Table 5 - Status Register (ADD = ‘1’)

Bit	Description
0	RXF#
1	TXE#
2	-
3	-
4	RXF IRQEn
5	TXE IRQEn
6	-
7	-

3. VDRIVE2 Dimensions

Figure 5 - VDRIVE2 mechanical dimensions



Fully detailed mechanical drawings for the VDrive2 enclosure are available on request from FTDI technical support.

4. Application Example - VDRIVE2 to PIC Micro Interface

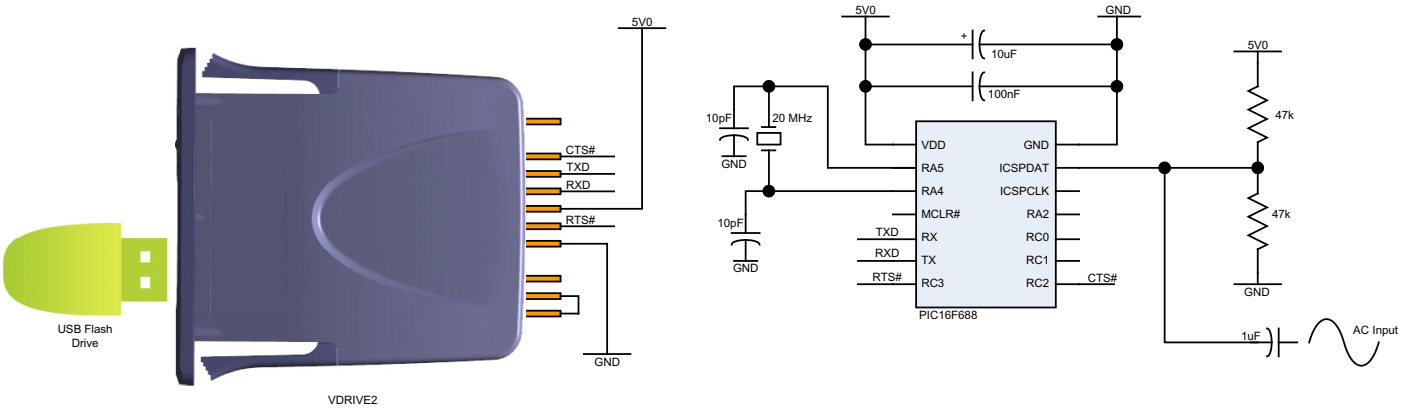


Figure 6 - Datalogging to a USB Flash disk with the VDrive2

By adding a PIC microcontroller and a few other components, the VDRIVE2 module can be turned into a Flash disk based data logger. Fig 5 shows the schematic of this simple application. The AC signal input is connected to the 10-bit analogue to digital converter on board the Microchip PIC. The PIC code takes a pre-defined number of samples and then writes the corresponding ASCII values to a comma separated value (CSV) file on the USB flash disk attached to the VDRIVE2 module. Vinculum's DOS like ASCII commands simplify the task of file handling. An extended ASCII command set is designed for use with a terminal whilst a shortened hexadecimal version is used with a microcontroller.

Consult the Vinculum VDAP firmware datasheet for full details of the command set used by the VDrive2.

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